Chettinad College of Engineering & Technology
Approved by AICTE, New Delhi and Affiliated to Anna University, Chennai.

Department of Electronics and Communication Engineering

EC8095 – VLSI DESIGN

Unit II - MCQ Bank

1. Register transfer level description specifies all of the registers in a design & _____ logic between them.

a. Sequential

b. Combinational

c. Both a and b

d. None of the above

ANSWER: b

2. The power consumption of static CMOS gates varies with the _____ of power supply voltage.

a. Square

b. Cube

c. Fourth power

d. 1/8th power

ANSWER: a

3.In CMOS logic circuit, the switching operation occurs because:

a) Both n-MOSFET and p-MOSFET turns OFF simultaneously for input '0' and turns ON simultaneously for input '1'

b) Both n-MOSFET and p-MOSFET turns ON simultaneously for input '0' and turns OFF simultaneously for input '1'

c) N-MOSFET transistor turns ON, and p-MOSFET transistor turns OFF for input '1' and N-MOS transistor turns OFF, and p-MOS transistor turns ON for input '0'

d) None of the mentioned

ANSWER: c

4. In CMOS logic circuit the n-MOS transistor acts as:

a) Load

b) Pull up network

c) Pull down network

d) Not used in CMOS circuits

ANSWER: c

5. In CMOS logic circuit the p-MOS transistor acts as:

a) Pull down network

b) Pull up network

c) Load

d) Short to ground

ANSWER: b

6.**The truth table which accurately explains the operation of CMOS not gate is:**

a)

Input	pMOS	nMOS	Output
0	OFF	ON	1
1	OFF	ON	0

b)

Input	pMOS	nMOS	Output
0	ON	OFF	1
1	ON	OFF	0

c)

Input	pMOS	nMOS	Output
0	ON	ON	1
1	OFF	OFF	0

d)

Input	pMOS	nMOS	Output
0	ON	OFF	1
1	OFF	ON	0

Answer: d

7. The input signal combination in exhaustive testing is given as

a) 2^N

b) $2^{1/N}$

c) $2^{(M+N)}$

d) $1/2^{N}$

Answer: a

8. The power dissipation in Pseudo-nMOS is reduced to about compared to nMOS device ----------

a) 50%

b) 30%

c) 60%

d) 70%

Answer: c

9. In dynamic CMOS logic is used ----------

a) Two phase clock

b) Three phase clock

c) One phase clock

d) Four phase clock

Answer: d

10. In clocked CMOS logic, output in evaluated in ----------

a) On period

b) Off period

c) Both periods

d) Half of on period

Answer: a

11. In CMOS domino logic is used ----------

a) Two phase clock

b) Three phase clock

c) One phase clock

d) Four phase clock

Answer: c

12. CMOS domino logic is same as with inverter at the output line ----------

a) Clocked CMOS logic

b) Dynamic CMOS logic

c) Gate logic

d) Switch logic

Answer: b

13. In CMOS domino logic is possible ----------

a) Inverting structure

b) Non inverting structure

c) Inverting and non inverting structure

d) Very complex design

Answer: b

14. CMOS domino logic occupies ----------

a) Smaller area

b) Larger area

c) Both of the mentioned

d) None of the mentioned

Answer: a

15**. CMOS domino logic has ----------**

a) Smaller parasitic capacitance

b) Larger parasitic capacitance

c) Low operating speed

d) Very large parasitic capacitance

Answer: a

16**. For a pseudo nMOS design the impedance of pull up and pull down ratio is ----------**

a) 4:1

b) 1:4

c) 3:1

d) 1:3

Answer: c

17. In CMOS NAND gate, p transistors are connected in ----------

a) Series

b) Parallel

c) Cascade

d) Random

Answer: b

18. The CMOS inverter has power dissipation ----------

a) Low

b) More

c) No

d) Very less

Answer: c

19. Gate logic is also called as ----------

a) Transistor logic

b) Switch logic

c) Complementary logic

d) Restoring logic

Answer: d

20. Power dissipation in switch logic is ----------

a) Less

b) More

c) High

d) Very less

Answer: a

21. The switch logic approach takes static current ----------

a) Low

b) More

c) No

d) Very less

Answer: c

22. Switch logic is based on ----------

a) Pass transistors

b) Transmission gates

c) Pass transistors and transmission gates

d) Design rules

Answer: c

23. In dynamic CMOS logic is used ----------

a) Two phase clock

b) Three phase clock

c) One phase clock

d) Four phase clock

Answer: d

24. Pseudo-nMOS has higher pull-up resistance than nMOS device.

a) True

b) False

Answer: a

25. In Pseudo-nMOS logic, n transistor operates in ----------

a) Cut off region

b) Saturation region

c) Resistive region

d) Non saturation region

Answer: b